REMARKS

Claims 1-32 and 39-52 are pending in the application. Claims 33-38 have been canceled without prejudice. Claims 1 and 17 have been amended where the word "a" has been changed to the word "the" to correct the antecedent basis for the controlling I/O line. Favorable reconsideration of this application is respectfully requested in light of the above amendments and the following detailed discussion.

Interview

On October 27, 2005 a telephonic interview was held between Examiner Tammara R. Peyton and counsel for the applicants, Donald A. Schurr and Stephen G. Kimmet. It is applicants' position that all claims should be allowed since neither Curry, Slattery, nor Little teach the limitations of differences of instantaneous source impedance of the controlling I/O line. The Examiner has been unable to cite in Curry, Slattery, or Little where these limitations are taught.

In addition, other related topics discussed in the interview were protocols of the cited art and ratios of read impedance to write impedance of the claimed invention, where applicants' counsel referenced, for example, page 6, lines 13-20 of the present application. Applicants' counsel asserted that the claimed invention communicates by utilizing the differences of instantaneous source impedance of the controlling I/O line during data out and data in modes, over only a single I/O line (as independent claims 1

and 17 claim). On the other hand, Curry, Slattery, and Little do not disclose and are not concerned with ratios of read impedance to write impedance, since Curry, Slattery, and Little communicate by utilizing protocols during data out and data in modes, which are not instantaneous.

Claim Rejections – 35 U.S.C. § 102

The Examiner has rejected claims 1-5, 17, 20, 22, 25-32, 40, and 41 under 35 U.S.C. 102(b) as being anticipated by Curry et al., (U.S. Patent No. 5,761,697, hereinafter Curry).

The Examiner asserts that as per claims 1-5, 17, 20, 22, 25-32, 40, and 41, Curry teaches a circuit (2704) for controlling the direction of data traffic, between a first device (computer 2702, Fig. 27) and a second device (2712, 2714, Fig. 27), over only a single I/O line (2706, Fig. 27) by utilizing the differences of instantaneous source impedance of a controlling I/O line during data out and data in modes (Abstract, cols. 49-57).

The Examiner also asserts that, Curry teaches a circuit (2704) that controls the direction of data traffic between a first and second device via connected bus line that uses the differences of instantaneous source impedance that is changed between a low impedance and a high impedance. The Examiner concludes from this that it would have been inherent that controlling of input and output data communication is without

the presence of any additional signaling protocol that identifies a data input phase or a data output phase.

Applicants, however, assert that amended independent claims 1 and 17, from which, respectively, dependent claims 2-5 and dependent claims 20, 22, 25-32, 40, and 41 directly or indirectly depend, specifically require at least the limitations of utilizing the differences of instantaneous source impedance of the controlling I/O line. Applicants find that the Merriam-Webster Dictionary defines instantaneous to be "done, occurring, or acting without any perceptible duration of time."

The Examiner asserts that these limitations can be found in the Curry Abstract and at columns 49-57. However, after studying Curry, applicants can find nowhere in Curry where at least these limitations are taught or suggested. Instead, applicants find that Curry teaches a 1-wire protocol (see, for example, Abstract).

Attached hereto is Exhibit A which is the specification for the Dallas Semiconductor (i.e., Assignee of the Curry patent) DS2401 electronic device that employs what Dallas Semiconductor also refers to as the "1-wire protocol." On page 5 of Exhibit A, the 1-wire protocol is defined to be a strict protocol to ensure data integrity that consists of four types of signaling: reset sequence with Reset Pulse and Presence Pulse, write 0, write 1, and read data. All of these signals except the Presence Pulse are initiated by the "bus" master. This 1-wire protocol of Curry is contrary to the claimed invention that requires difference of instantaneous source impedance of the controlling I/O line, without requiring a bus master.

Also, applicants find at least the following time signals/delays (see, for example, page 5 of Exhibit A) that Curry's protocol requires: a) a Reset Pulse transmission of at least 480µs, b) after detecting the rising edge on the data pin the protocol waits 15-60µs, and c) then the protocol transmits the Presence Pulse of 60-240µs. In total, this "additional protocol" of Curry requires nearly a millisecond (therefore, Curry's protocol is not instantaneous) in which to operate and comprises "non-bit" overhead.

The present application teaches the differences between signaling protocols that are used, as in U.S. Patent No. 5,045,675 also to Curry for the half-duplex case, and U.S. Patent No. 5,729,547 to Dute' (see, for example, page 3, lines 19-29).

Also, the claimed invention, however, operates with no additional protocol (claim 3), without any non-bit overhead (claim 4), on a bit-by-bit basis (claim 20) that is independent of any signaling protocol (claims 22, 25-28), and without the need of timing commands and circuits (claims 29-32). Applicants can find nowhere in Curry where Curry teaches or suggests these additional limitations.

Therefore, applicants respectfully submit that independent claim 1 and claims 2-5 that depend directly or indirectly from claim 1, and independent claim 17 and claims 20, 22, 25-32, 40, and 41 that depend directly or indirectly from claim 17, are not anticipated by Curry, as the inventions defined thereby are not identically disclosed in Curry, as required by 35 U.S.C. § 102(b).

Consequently, claims 1-5, 17, 20, 22, 25-32, 40, and 41 should be allowed over Curry. Accordingly, withdrawal of the rejection of claims 1-5, 17, 20, 22, 25-32, 40, and

41, and favorable reconsideration of claims 1-5, 17, 20, 22, 25-32, 40, and 41, are respectfully requested.

Claim Rejections – 35 U.S.C. § 103

1. The Examiner has rejected claims 6-16, 18, 19-21, 23, 24, 39-42, 44-52 under 35 U.S.C. § 103(a) as being unpatentable over Curry.

The Examiner concedes that as per claims 6-9, 18, 19, Curry does not clearly teach wherein a ratio of said high impedance to said low impedance is about or at least 1000:1, 500:1, or 100:1 or between 1000:1 and 10000:1. The Examiner asserts that, however, it would have been obvious to one of ordinary skill that the ratio of high/low impedance of Curry's circuit could be modified to implement a host of other ratio, because, as the Examiner admits, doing so would ensure the practicality of Curry's circuit when implement in other systems.

The Examiner continues by asserting that as per claims 39 and 44-47, Curry teaches a peripheral circuit for controlling traffic data signals between a first and second device, therefore, it would have been obvious to one of ordinary skill that the adapter would ensure data is routed to the proper destination.

The Examiner continues by asserting that as per claims 10-16, 20, 21, 23, 24, 40, and 41, Curry disclosed the use of a microprocessor in a computer and a connected memory peripheral device and obvious control lines, therefore, it would have been

obvious that Curry's system could be implemented in other system thereby expanding the flexibility.

Next the Examiner concedes that as per claims 42 and 48-52, Curry does not teach a data signal and clock signal separation circuit for separation of data-out + clock and data-in at the peripheral device such that it can interface to a standard SPI device or a standard UART at the peripheral device, which is performed such that it can interface to devices which use Pulse Width Modulation to convey analog values. However, separation circuit and the use of Pulse Width Modulation to convey analog values are well known in the art, thereby making their use obvious to one of ordinary skill (cols. 32-34).

Applicants, however, assert that since amended independent claims 1 and 17 are patentable over Curry, then dependent claims 6-16 and dependent claims 18, 19-21, 23, 24, 39-42, 44-52, which, respectively, depend directly or indirectly from claims 1 and 17, are also patentable, at least on this basis.

In this 35 U.S.C. § 103(a) rejection, the Examiner concedes that as per claims 6-9 (applicants note that claim 14 also requires these limitations), 18, and 19, Curry does not clearly teach, wherein a ratio of said high impedance to said low impedance is about or at least 1000:1, 500:1, or 100:1 or between 1000:1 and 10000:1. Notwithstanding these concessions, the Examiner rejects these claims as unpatentable over Curry alone.

Applicants, however, assert that the above-noted ratios (i.e., the ratios of the read (high impedance) to the write (low impedance)) are distinguishing limitations of applicants' discovery (see, for example, page 6, lines 13-20). Applicants agree with the Examiner's admission of the practicality of these limitations, which the Examiner concedes that Curry does not clearly teach. Applicants assert that these limitations, which Curry makes no mention of, are not obvious.

Therefore, applicants assert that according to the MPEP, "[t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references, when combined) must teach or suggest all the claim limitations." See MPEP 2143 (emphasis added). Thus, MPEP 2143.03 specifically states that, "to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974) (emphasis supplied).

Thus, applicants assert that Curry falls to teach or suggest all the claim limitations (e.g., utilizing the differences of instantaneous source impedance of the controlling I/O line, and/or the ratio of said high impedance to said low impedance is about or at least 1000:1, 500:1, or 100:1 or between 1000:1 and 10000:1), and the mere allegation that the differences between the claimed subject matter and the prior

art are obvious does not support a prima facie case of unpatentability. See *In re Soli*, 137 USPQ 797 (CCPA 1963).

In addition, the claimed invention operates on a bit-by-bit basis (claim 20). Applicants can find nowhere in Curry where Curry teaches or suggests these additional limitations.

Therefore, claims 6-16, 18-21, 23, 24, 39-42, and 44-52 are patentable over Curry, as the inventions defined thereby are not suggested within Curry nor is there any suggestion or motivation to modify this reference's teachings in order to teach or suggest the claimed limitations, as required by 35 U.S.C. § 103. Consequently, claims 6-16, 18, 23, 24, 39-42, and 44-52 should be allowed over Curry. Accordingly, favorable reconsideration of claims 6-16, 18, 23, 24, 39-42, and 44-52 are respectfully requested.

2. The Examiner has rejected claims 1-9, 14-16, 39, 42, and 44-52 under 35 U.S.C. 103(a) as being unpatentable over Slattery et al. (U.S. Patent No. 5,361,005, hereinafter Slattery).

The Examiner admits that, as per claims 1-5, Slattery teaches a circuit (312) for "controlling" the direction of data traffic, between a first device (304, Fig. 3) and a second device (308, Fig. 3), over only a single I/O line (301, Fig. 3), but asserts by utilizing the differences of instantaneous source impedance (low or high) of a controlling I/O line during data out and data in modes (Abstract, cols. 2-6).

The Examiner continues by conceding that Slattery teaches a peripheral circuit (312) that "controls" the direction of data traffic between a first and second device via connected "bus line", but then asserts that this control utilizes the differences of instantaneous source impedance that is changed between a low impedance and a high impedance. The Examiner continues by asserting that it would have been obvious to one of ordinary skill that the controlling of input and output data communication is without the presence of any additional signaling protocol that identifies a data input phase or a data output phase.

The Examiner concedes that as per claims 6-9, Slattery does not clearly teach wherein a ratio of said high impedance to said low impedance is about or at least 1000:1, 500:1, or 100:1 or between 1000:1 and 10000:1, however, it would have been obvious to one of ordinary skill that the ratio of high/low impedance of Kniess' (sic, applicants assume the Examiner means Slattery's) adapter could be modified to implement a host of other radio (sic, assume ratios), because doing so would ensure the practicality of Kniess' (sic, assume Slattery's) adapter when implemented in other systems.

The Examiner asserts that as per claims 39 and 44-47, Slattery teaches a peripheral circuit for controlling traffic data signals between a first and second device, therefore, it would have been obvious to one of ordinary skill that the adapter would ensure data is routed to the proper destination.

The Examiner asserts that as per claims 14-16, Slattery disclosed in a prior art system the use of a microprocessor and a memory peripheral device and obvious control lines, therefore, it would have been obvious that Slattery's system could be implemented in other systems thereby expanding the flexibility.

The Examiner concedes that as per claims 42 and 48-52, Slattery does not teach a data signal and clock signal separation circuit for separation of data-out + clock and data-in at the peripheral device such that it can interface to a standard SPI device or a standard UART at the peripheral device, which is performed such that it can interface to devices which use Pulse Width Modulation to convey analog values. The Examiner concludes from this that, however, separation circuit and the use of Pulse Width Modulation to convey analog values are well known in the art, thereby making their use obvious to one of ordinary skill.

Applicants, however, assert that amended independent claims 1 and 17, from which, respectively, dependent claims 2-9 and 14-16 and dependent claims 39, 42, and 44-52 depend directly or indirectly, specifically require at least the limitations of utilizing the differences of instantaneous source impedance of the controlling I/O line, not just low and high impedance as the Examiner asserts.

After studying the Slattery patent, applicants can find nowhere in Slattery where at least these limitations are taught or suggested. Instead, applicants find that Slattery teaches a driver/termination circuit having a logic circuit that defines operating modes.

The logic circuit can be changed by command from a host computer or automatically selected by a peripheral device (see, for example, Abstract).

In other words, Slattery teaches a "control" circuit 312 (which is a driver circuit (e.g., computer 304) / termination (e.g., peripheral device 310)) that allows either the computer to place the circuit 312 in one of three modes (see, for example, column 4, at lines 5-8) or the peripheral device to automatically change modes to minimize errors (see, for example, column 4, at lines 40-45) by way of the logic circuit (see, for example, Fig. 3).

Slattery is silent on utilizing the differences of instantaneous source impedance of the controlling I/O line. Instead, the Slattery control circuit 312 communicates between a peripheral (for example, a floppy disk drive) and an IBM PC-AT or PS/2 via a controller bus (see, for example, Abstract and column 1, lines 7-21). Such buses (circa 1993) are anything but instantaneous that utilize "slow protocols", which are contrary to the claimed invention.

Further, applicants assert that the above-noted ratios (i.e., the ratios of the read to the write) are distinguishing limitations of applicants' discovery. Also, applicants agree with the Examiner's admission of the practicality of these limitations, which the Examiner admits that Slattery clearly does not teach. Applicants, however, assert that these limitations, which Slattery makes no mention of, are not obvious.

Therefore, applicants refer to the above referenced MPEP 2143 that requires, "to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art."

Specifically, Slattery does not teach ratios as required by claims 6-9 and 14. The circuit modes of Slattery are commanded by a host computer or selected by a peripheral device via a bus (that requires a protocol), whereas claim 3 operates with no additional protocol and claim 4 without any non-bit overhead.

Therefore, claims 1-9, 14-16, 39, 42, and 44-52 are patentable over Slattery, as the inventions defined thereby are not suggested within Slattery nor is there any suggestion or motivation to modify this reference's teachings in order to teach or suggest the claimed limitations, as required by 35 U.S.C. § 103. Consequently, claims 1-9, 14-16, 39, 42, and 44-52 should be allowed over Slattery. Accordingly, favorable reconsideration of claims 1-9, 14-16, 39, 42, and 44-52 are respectfully requested.

3. The Examiner has rejected claims 1-32 and 39-52 under 35 U.S.C. 103(a) as being unpatentable over Little et al., (U.S. Patent No. 6,412,072).

The Examiner asserts that as per claims 1-5, 10-17, 20-32, 40, and 41 Little teaches a circuit for "controlling" the direction of data traffic, between a first device (Fig. 2) and a second device (Fig. 2), over only a single I/O line by utilizing the differences of instantaneous source impedance (low or high) of a controlling I/O line during data out and data in modes (Abstract, cols. 2-39).

The Examiner asserts that Little teaches a circuit that controls the direction of data traffic between a first and second device via connected bus line that uses the differences of instantaneous source impedance that is changed between a low impedance and a high impedance. The Examiner concludes from this that it would have been obvious to one of ordinary skill that the controlling of input and output data communication is without the presence of any additional signaling protocol that identifies a data input phase or a data output phase.

The Examiner admits that as per claims 6-9, 18, 19, Little does not clearly teach wherein a ratio of said high impedance to said low impedance is about or at least 1000:1, 500:1, or 100:1 or between 1000:1 and 10000:1. The Examiner concludes from this, however, it would have been obvious to one of ordinary skill that the radio of high/low impedance of Little circuit could be modified to implement a host of other ratio, because doing so would ensure the practicality of Little's circuit when implement (sic) in other systems.

The Examiner asserts that as per claims 39 and 44-47, Little teaches a peripheral circuit for controlling traffic data signals between a first and second device, therefore, it would have been obvious to one of ordinary skill that the adapter would ensure data is routed to the proper destination.

The Examiner admits that as per claims 42, 48, and 49-52, Little does not teach a data signal and clock signal separation circuit for separation of data-out + clock and data-In at the peripheral device such that it can interface to a standard SPI device or a

standard UART at the peripheral device, which is performed such that it can interface to devices which use Pulse Width Modulation to convey analog values. The Examiner concludes from this that, however, separation circuit and the use of Pulse Width Modulation to convey analog values are well known in the art, thereby making their use obvious to one of ordinary skill.

Applicants, however, assert that amended independent claims 1 and 17, from which, respectively, dependent claims 2-16 and dependent claims 18-32 and 39-52 directly or indirectly depend, specifically require at least the limitations of utilizing the differences of instantaneous source impedance of the controlling I/O line. As noted above, applicants find that the Merriam-Webster Dictionary defines instantaneous to be "done, occurring, or acting without any perceptible duration of time."

After studying Little, applicants can find nowhere in Little where at least these limitations are taught or suggested. Instead, applicants find that Little teaches a 1-wire protocol (see, for example, Abstract).

As noted above, Exhibit A is a copy of the specification for the Dallas Semiconductor (i.e., who is also the Assignee of the Little patent) DS2401 electronic device that employs the "1-wire protocol" of Little. On page 5 of Exhibit A, the 1-wire protocol is defined to be a strict protocol to ensure data integrity that consists of four types of signaling: reset sequence with Reset Pulse and Presence Pulse, write 0, write 1, and read data. All of these signals except the Presence Pulse are initiated by the bus master. This 1-wire protocol of Little is contrary to the claimed invention that

requires difference of instantaneous source impedance of the controlling I/O line, but requires no bus master to initiate said pulses.

Also, applicants find at least the following time signals/delays (see, for example, page 5 of Exhibit A) that Little's protocol requires: a) a Reset Pulse transmission of at least 480µs, b) after detecting the rising edge on the data pin the protocol waits 15-60µs, and c) then the protocol transmits the Presence Pulse of 60-240µs. In total, this "additional protocol" of Little requires nearly a millisecond (therefore, is not instantaneous) in which to operate and comprises "non-bit" overhead.

The claimed invention, however, operates with no additional protocol (claim 3), without any non-bit overhead (claim 4), on a bit-by-bit basis (claim 20) that is independent of any signaling protocol (claims 22, 25-28), and without the need of timing commands and circuits (claims 29-32). Applicants can find nowhere in Little where Little teaches or suggests these additional limitations.

In this 35 U.S.C. § 103(a) rejection, the Examiner concedes that as per claims 6-9, (applicants note that claim 14 also requires these limitations), 18, and 19, Little does not clearly teach, wherein a ratio of said high impedance to said low impedance is about or at least 1000:1, 500:1, or 100:1 or between 1000:1 and 10000:1). The Examiner then rejects these claims as unpatentable over Little alone.

Applicants, however, assert that the above-noted ratios (i.e., the ratios of the read to the write) are distinguishing limitations of applicants' discovery (see, for example, page 6, lines 13-20). Also, applicants agree with the Examiner's admission of

the practicality of these limitations, which the Examiner concedes that Little clearly does not teach. Applicants, however, assert that these limitations, which Little makes no mention of, are not obvious.

Therefore, applicants refer to the above referenced MPEP 2143 that requires, "to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art."

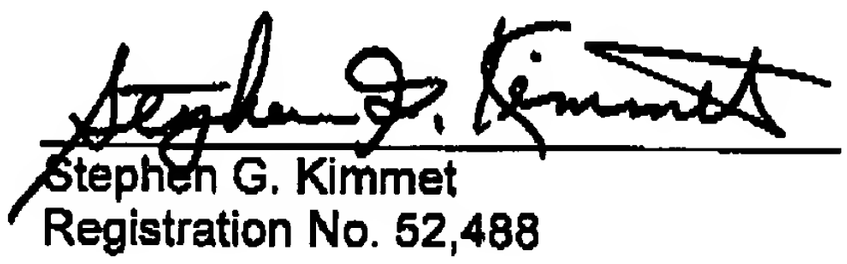
In addition, the claimed invention operates on a bit-by-bit basis (claim 20). Applicants can find nowhere in Little where Little teaches or suggests these additional limitations.

Therefore, claims 1-32 and 39-52 are patentable over Little, as the inventions defined thereby are not suggested within Little nor is there any suggestion or motivation to modify this reference's teachings in order to teach or suggest the claimed limitations, as required by 35 U.S.C. § 103. Consequently, claims 1-32 and 39-52 should be allowed over Little. Accordingly, favorable reconsideration of claims 1-32 and 39-52 are respectfully requested.

CONCLUSION

If the Examiner has any remaining questions or concerns, or would prefer claim language different from that included herein, the favor of a telephone call to the applicants' attorneys/agent is requested.

Respectfully submitted,



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--- EXHIBIT A ---

Appl. No. 09/916,215
Amdt. Dated November 9, 2005
Reply to Office Action of July 14, 2004

DALLAS SEMICONDUCTOR

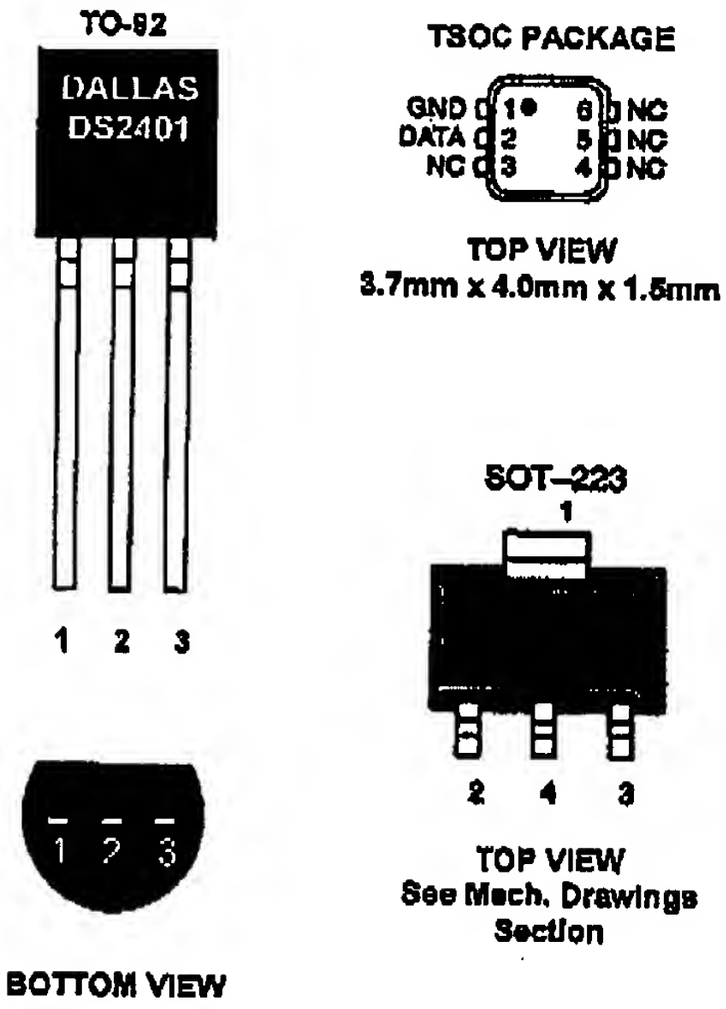
www.maxim-ic.com

DS2401
Silicon Serial Number

FEATURES

- Upgrade and drop-in replacement for DS2400
  - — Extended 2.8 to 6.0 voltage range
  - — Multiple DS2401s can reside on a common 1-Wire® Net
- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester); guaranteed no two parts alike
- Built-in multidrop controller ensures compatibility with other 1-Wire Net products
- 8-bit family code specifies DS2401 communications requirements to reader
- Presence Pulse acknowledges when the reader first applies voltage
- Low-cost TO-92, SOT-223, and TSOC surface mount packages
- Reduces control, address, data, and power to a single pin
- Zero standby power required
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3kbits/s
- TO-92 Tape & Reel version with leads bent to 100mil spacing (default) or with straight leads (DS2401T-SL)
- Applications
  - — PCB Identification
  - — Network Node ID
  - — Equipment Registration
- Operates over industrial temperature range of -40°C to +85°C

PIN ASSIGNMENT



PIN DESCRIPTION

	TO-92/SOT-223	TSOC
Pin 1	Ground	Ground
Pin 2	Data (DQ)	Data (DQ)
Pin 3	No Connect	No Connect
Pin 4	Ground	No Connect
Pin 5-6	–	No Connect

ORDERING INFORMATION

DS2401	TO-92 Package
DS2401Z	SOT-223 Surface Mount Package
DS2401/T&R	Tape & Reel of DS2401
DS2401T-SL	Like DS2401T but Straight Leads
DS2401Z/T&R	Tape & Reel of DS2401Z
DS2401P	TSOC Surface Mount Package
DS2401P/T&R	Tape & Reel of DS2401P
DS2401X1	Chip Scale Pkg., Tape & Reel

1-Wire is a registered trademark of Dallas Semiconductor.

DESCRIPTION

The DS2401 enhanced Silicon Serial Number is a low-cost, electronic registration number that provides an absolutely unique identity which can be determined with a minimal electronic interface (typically, a single port pin of a microcontroller). The DS2401 consists of a factory-lasered, 64-bit ROM that includes a unique 48-bit serial number, an 8-bit CRC, and an 8-bit Family Code (01h). Data is transferred serially via the 1-Wire protocol that requires only a single data lead and a ground return. Power for reading and writing the device is derived from the data line itself with no need for an external power source. The DS2401 is an upgrade to the DS2400. The DS2401 is fully reverse-compatible with the DS2400 but provides the additional multi-rop capability that enables many devices to reside on a single data line. The familiar TO-92, SOT-223 or TSOC package provides a compact enclosure that allows standard assembly equipment to handle the device easily.

OPERATION

The DS2401's internal ROM is accessed via a single data line. The 48-bit serial number, 8-bit family code and 8-bit CRC are retrieved using the Dallas 1-Wire protocol. This protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master. All data is read and written least significant bit first.

1-WIRE BUS SYSTEM

The 1-Wire bus is a system which has a single bus master system and one or more slaves. In all instances, the DS2401 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal type and timing). For a more detailed protocol description, refer to Chapter 4 of the *Book of DS19xx iButton® Standards*.

Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have an open-drain connection or 3-state outputs. The DS2401 is an open-drain part with an internal circuit equivalent to that shown in Figure 2. The bus master can be the same equivalent circuit. If a bidirectional pin is not available, separate output and input pins can be tied together. The bus master requires a pullup resistor at the master end of the bus, with the bus master circuit equivalent to the one shown in Figure 3. The value of the pullup resistor should be approximately 5kΩ for short line lengths. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The 1-Wire bus has a maximum data rate of 16.3kbits per second.

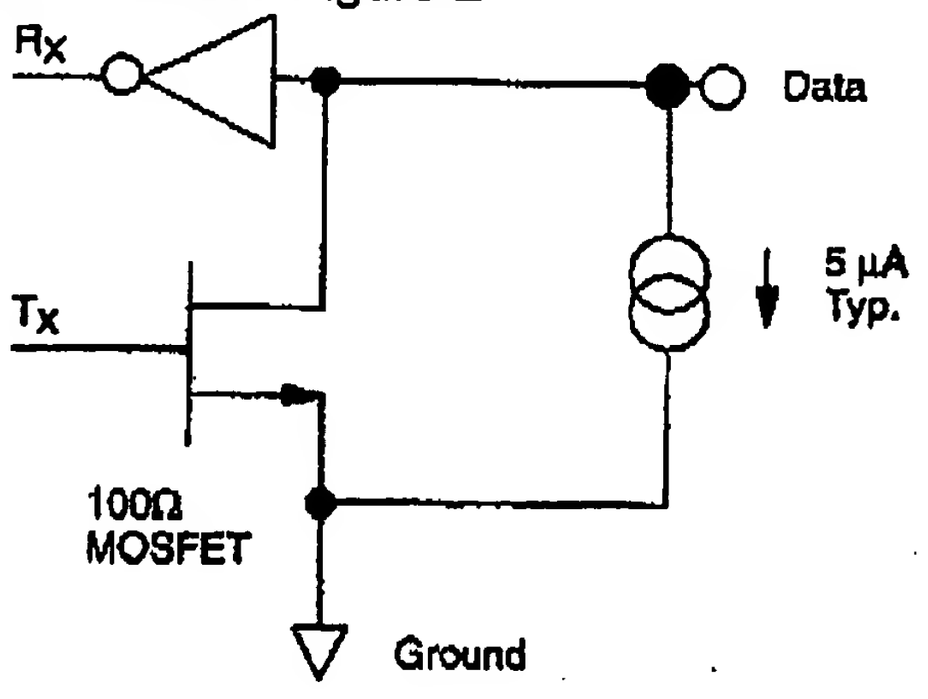
The idle state for the 1-Wire bus is high. If, for any reason, a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120µs, one or more of the devices on the bus may be reset.

DS2401 MEMORY MAP Figure 1

8-Bit CRC Code	48-Bit Serial Number	8-Bit Family Code (01h)
MSB LSB	MSB LSB	MSB LSB

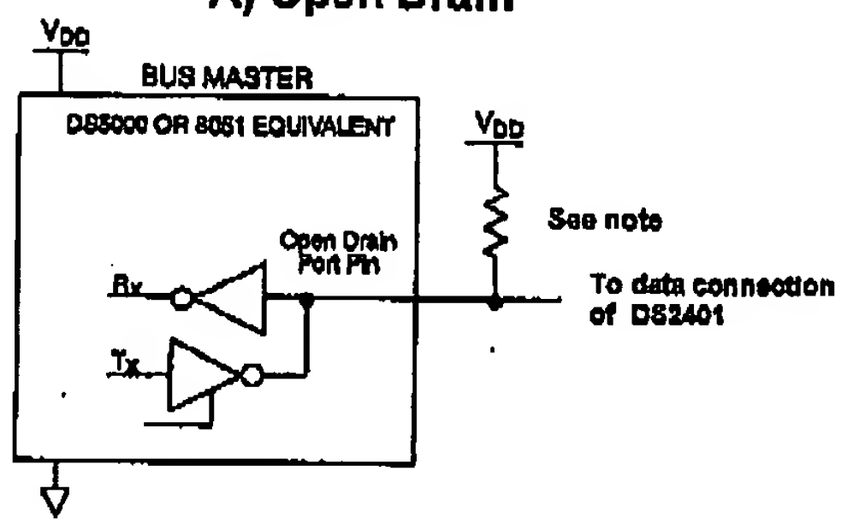
iButton is a registered trademark of Dallas Semiconductor.

DS2401 EQUIVALENT CIRCUIT Figure 2

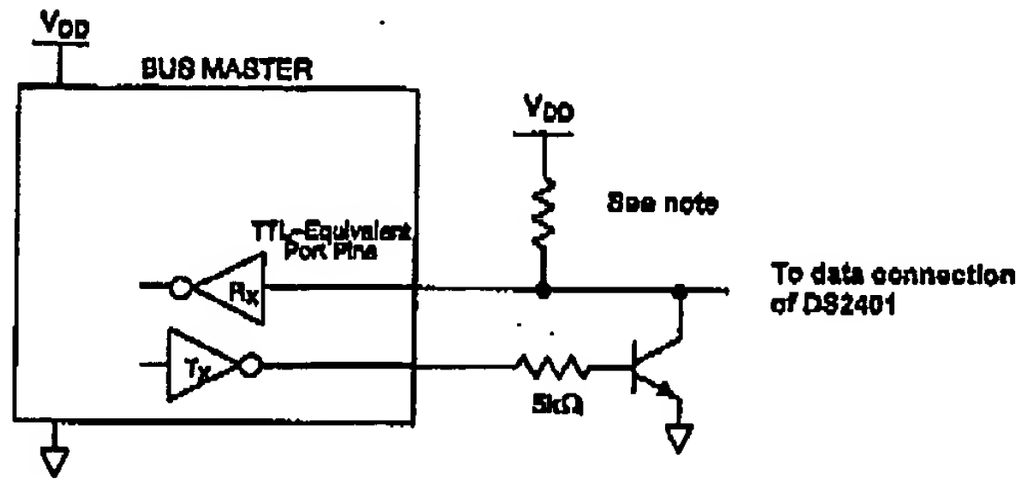


BUS MASTER CIRCUIT Figure 3

A) Open Drain



B) Standard TTL



Note:
Depending on the 1-Wire communication speed and the bus load characteristics, the optimal pullup resistor (R_{PU}) value will be in the 1.5kΩ to 5kΩ range.

TRANSACTION SEQUENCE

The sequence for accessing the DS2401 via the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Read Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a Presence Pulse(s) transmitted by the slave(s).

The Presence Pulse lets the bus master know that the DS2401 is on the bus and is ready to operate. For more details, see the 1-Wire Signaling section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are 8 bits long. A list of these commands follows (refer to flowchart in Figure 4):

Read ROM [33h] or [0Fh]

This command allows the bus master to read the DS2401's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS2401 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The DS2401 Read ROM function will occur with a command byte of either 33h or 0Fh in order to ensure compatibility with the DS2400, which will only respond to a 0Fh command word with its 64-bit ROM data.

Match ROM [55h] / Skip ROM [CCh]

The complete 1-Wire protocol for all Dallas Semiconductor iButtons contains a Match ROM and a Skip ROM command. (See the *Book of DS19xx iButton Standards.*) Since the DS2401 contains only the 64-bit ROM with no additional data fields, the Match ROM and Skip ROM are not applicable and will cause no further activity on the 1-Wire bus if executed. The DS2401 does not interfere with other 1-Wire parts on a multidrop bus that do respond to a Match ROM or Skip ROM (for example, a DS2401 and DS1994 on the same bus).

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The ROM search process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the *Book of DS19xx iButton Standards* for a comprehensive discussion of a ROM search, including an actual example.

1-WIRE SIGNALING

The DS2401 requires a strict protocol to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with Reset Pulse and Presence Pulse, write 0, write 1, and read data. All these signals except Presence Pulse are initiated by the bus master.

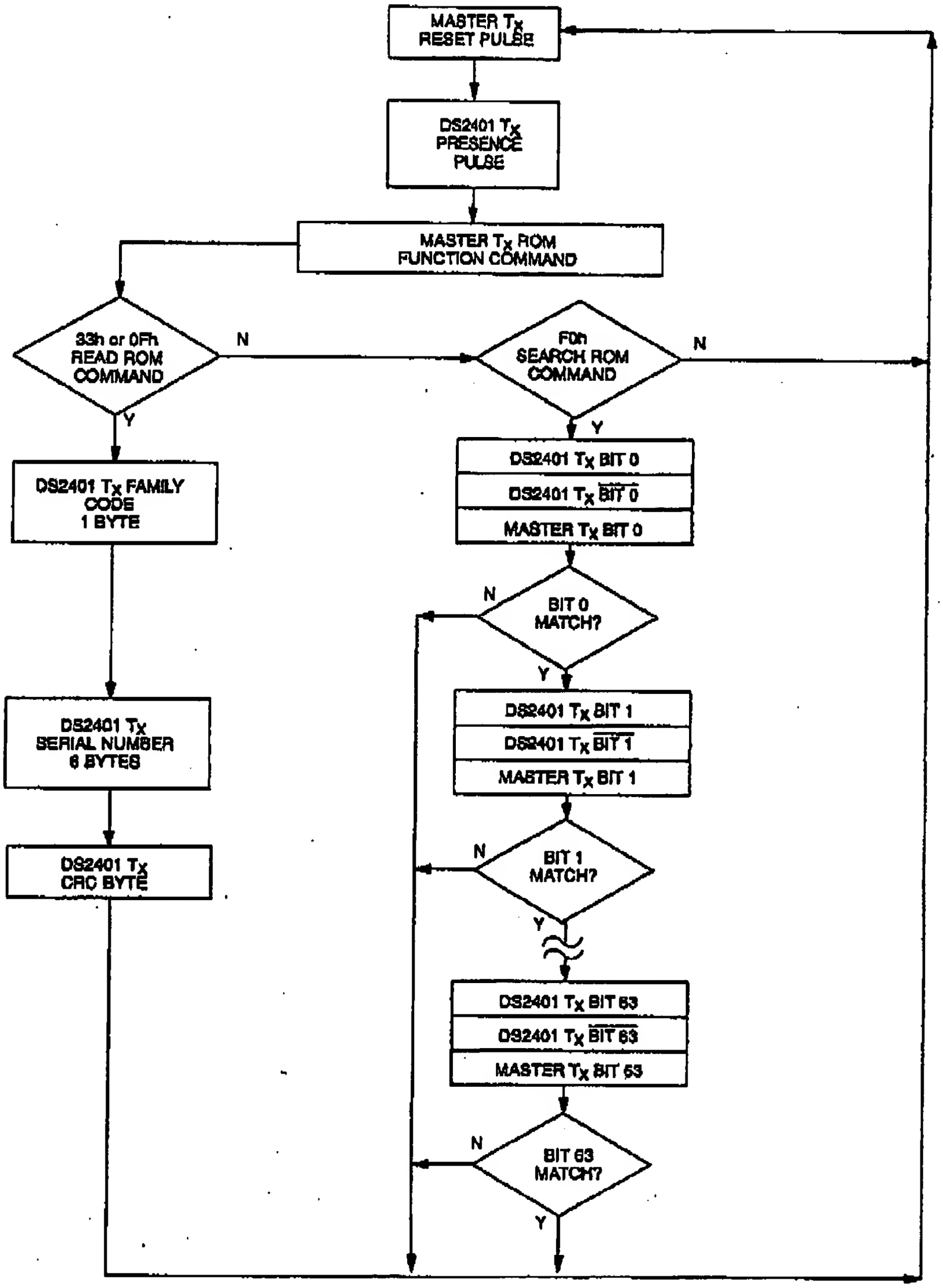
The initialization sequence required to begin any communication with the DS2401 is shown in Figure 5. A reset pulse followed by a Presence Pulse indicates the DS2401 is ready to send or receive data given the correct ROM command.

The bus master transmits (T_X) a reset pulse (t_{RSTL}, minimum 480µs). The bus master then releases the line and goes into receive mode (R_X). The 1-Wire bus is pulled to a high state via the 5kΩ pullup resistor. After detecting the rising edge on the data pin, the DS2401 waits (t_{PDH}, 15-60µs) and then transmits the Presence Pulse (t_{PDL}, 60-240µs). The 1-Wire bus requires a pullup resistor range of 1.5kΩ to 5kΩ, depending on bus load characteristics.

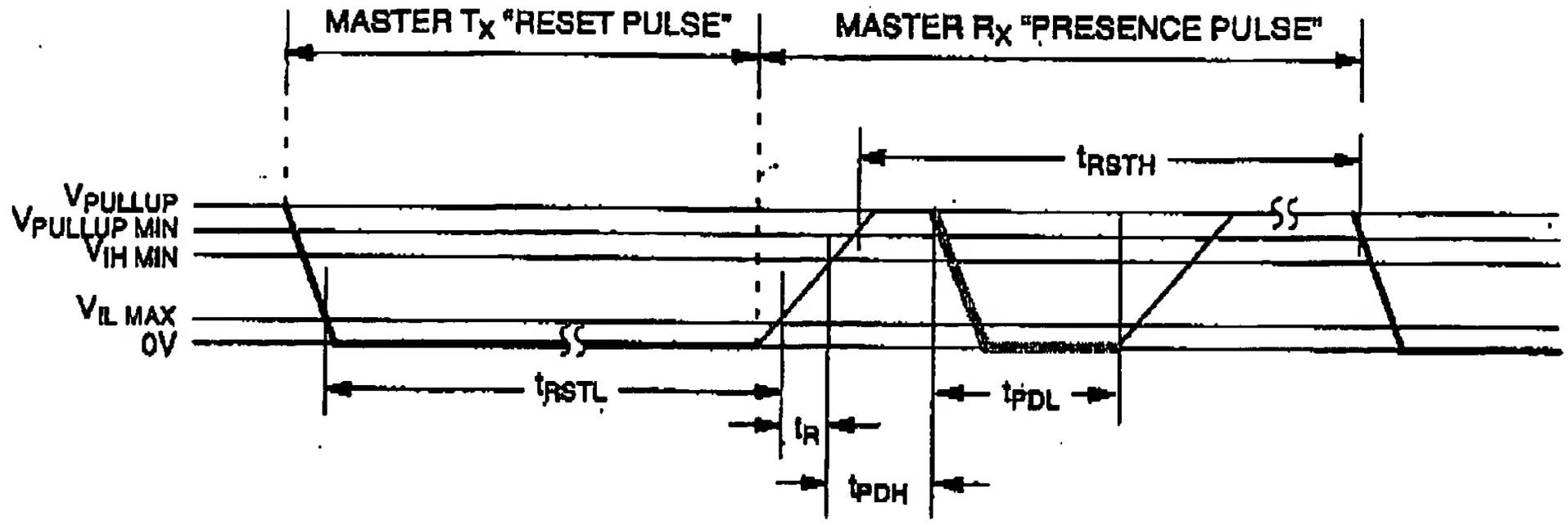
READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 6. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS2401 to the master by triggering a delay circuit in the DS2401. During write time slots, the delay circuit determines when the DS2401 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS2401 will hold the data line low overriding the "1" generated by the master. If the data bit is a 1, the DS2401 will leave the read data time slot unchanged.

ROM FUNCTIONS FLOW CHART Figure 4



INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 5

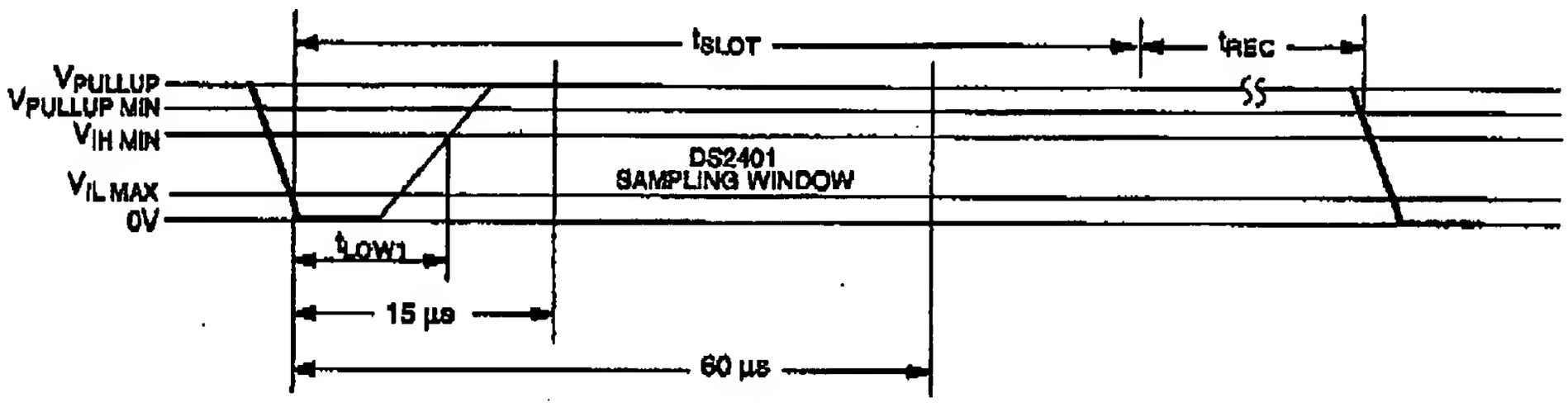


RESISTOR	$480\mu s \le t_{RSTL} < \infty$ *
MASTER	$480\mu s \le t_{RSTH} < \infty$ (includes recovery time)
DS2401	$15\mu s \le t_{PDH} < 60\mu s$
	$60\mu s \le t_{PDL} < 240\mu s$

* In order not to mask interrupt signaling by other devices on the 1-Wire bus, $t_{RSTL} + t_R$ should always be less than 960µs.

READ/WRITE TIMING DIAGRAM Figure 6

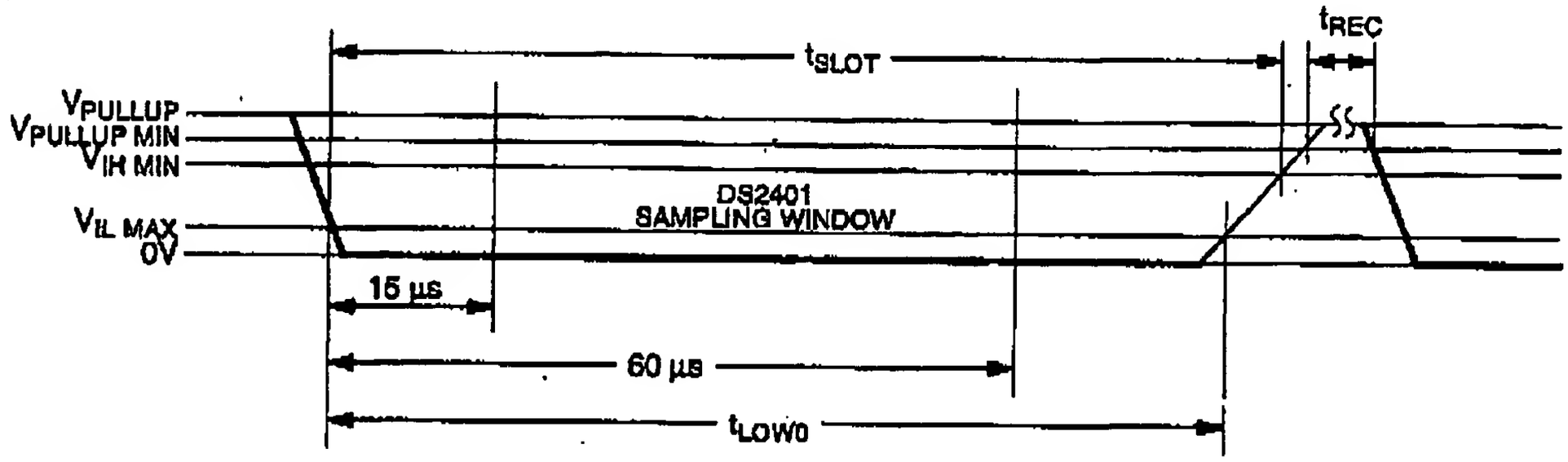
Write-One Time Slot



RESISTOR	$60\mu s \le t_{SLOT} < 120\mu s$
MASTER	$1\mu s \le t_{LOW1} < 15\mu s$
	$1\mu s \le t_{REC} < \infty$

READ/WRITE TIMING DIAGRAM (cont'd) Figure 6

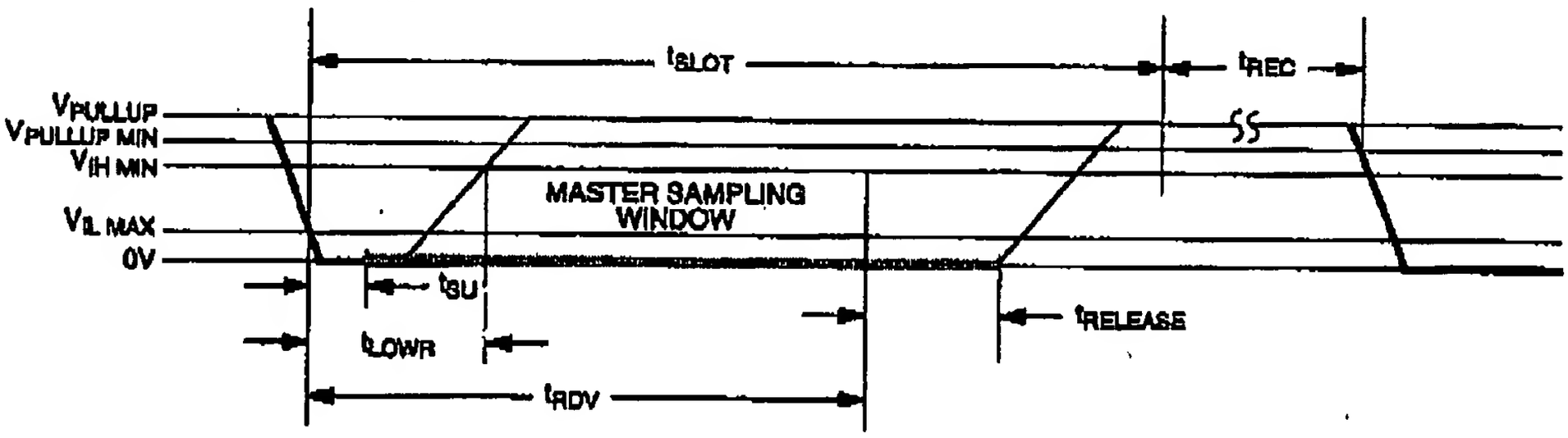
Write-zero Time Slot

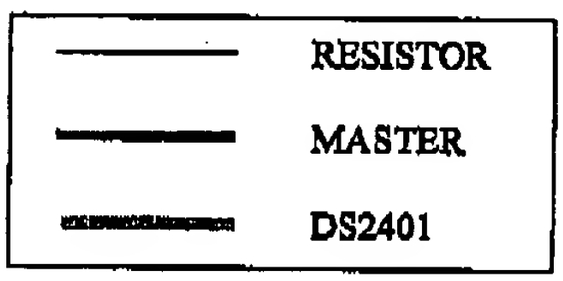


$60\mu s \le t_{LOW0} < t_{SLOT} < 120\mu s$

$1\mu s \le t_{REC} < \infty$

Read-data Time Slot





$60\mu s \le t_{SLOT} < 120\mu s$
$1\mu s \le t_{LOWR} < 15\mu s$
$0 \le t_{RELEASE} < 45\mu s$
$1\mu s \le t_{REC} < \infty$
$t_{RDV} = 15\mu s$
$t_{SU} < 1\mu s$

CRC GENERATION

To validate the data transmitted from the DS2401, the bus master may generate a CRC value from the data as it is received. This generated value is compared to the value stored in the last 8 bits of the DS2401. If the two CRC values match, the transmission is error-free.

The equivalent polynomial function of this CRC is: $CRC = x^8 + x^5 + x^4 + 1$. For more details, see the *Book of DS19xx iButton Standards*.

CUSTOM DS2401

Customization of a portion of the unique 48-bit serial number by the customer is available. Dallas Semiconductor will register and assign a specific customer ID in the 12 most significant bits of the 48-bit field. The next most significant bits are selectable by the customer as a starting value, and the least significant bits are non-selectable and will be automatically incremented by one. Certain quantities and conditions apply for these custom parts. Contact your Dallas Semiconductor sales representative for more information.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See J-STD-020A Specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{PUP} = 2.8V to 6.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1,6
Logic 0	V_{IL}	-0.3		+0.8	V	1, 11
Output Logic Low @ 4 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1,2
Input Load Current	I_L		5		µA	3
Operating Charge	Q_{OP}			30	nC	7,8

CAPACITANCE

(t_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
I/O (1-Wire)	$C_{IN/OUT}$			800	pF	9

AC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{PUP} = 2.8V to 6.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	13
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Data Valid	t_{RDV}		15		µs	12
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480		960	µs	10
Presence Detect High	t_{PDH}	15		60	µs	
Presence Detect Low	t_{PDL}	60		240	µs	

NOTES:

1) All voltages are referenced to ground.

2) V_{PUP} = external pullup voltage.

3) Input load is to ground.

4) An additional reset or communication sequence cannot begin until the reset high time has expired.

5) Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1µs of this falling edge and will remain valid for 14µs minimum (15µs total from falling edge on 1-Wire bus).

6) V_{IH} is a function of the external pullup resistor and the V_{CC} supply.

7) 30 nanocoulombs per 72 time slots @ 5.0V.

8) At V_{CC} = 5.0V with a 5kΩ pullup to V_{CC} and a maximum time slot of 120µs.

9) Capacitance on the I/O pin could be 800pF when power is first applied. If a 5kΩ resistor is used to pullup the I/O line to V_{CC}, 5µs after power has been applied the parasite capacitance will not affect normal communications.

10) The reset low time (t_{RSTL}) should be restricted to a maximum of 960µs, to allow interrupt signaling, otherwise it could mask or conceal interrupt pulses if this device is used in parallel with a DS2404 or DS1994.

11) Under certain low voltage conditions, V_{ILMAX} may have to be reduced to as much as 0.5V to always guarantee a Presence Pulse.

12) The optimal sampling point for the master is as close as possible to the end time of the t_{RDV} period without exceeding t_{RDV}. For the case of a Read-One Time slot, this maximizes the amount of time for the pullup resistor to recover to a high level. For a Read-Zero Time slot, it ensures that a read will occur before the fastest 1-Wire device(s) releases the line.

13) The duration of the low pulse sent by the master should be a minimum of 1µs with a maximum value as short as possible to allow time for the pullup resistor to recover the line to a high level before the 1-Wire device samples in the case of a Write-One Time or before the master samples in the case of a Read-One Time.